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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No.: RPS920010005US1

In re Application of: §	
§	
RENGAN ET AL. §	
§	Examiner: NGUYEN, K.
Serial No.: 09/904,622 §	
§	Art Unit: 2677
Filed: 13 JULY 2001 §	
§	
For: **DISPLAY PRIVACY FOR** §	
ENHANCED PRESENTATIONS WITH §	
REAL-TIME UPDATES §	

APPEAL BRIEF

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The present Appeal Brief is submitted in support of the Appeal in the above-identified application.

The fee for the submission of an Appeal Brief has been paid for under the previous appeal, and no additional fee or extension of time is believed to be required. However, in the event any additional fee or extension of time is required, please charge that fee to the Lenovo (US) Deposit Account 50-3533.

CERTIFICATE OF FACSIMILE TRANSMISSION
37 CFR § 1.8(a)

I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office via facsimile on the date below.

5/15/06
Date

Signature

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REAL PARTY IN INTEREST

The present application is assigned to Lenovo Incorporation, the real party of interest.

RELATED APPEALS AND INTERFERENCES

No related appeal is presently pending.

STATUS OF THE CLAIMS

Claims 1-15, which were finally rejected by the Examiner as noted in the Final Office Action dated March 29, 2006 and in the Advisory Action dated May 2, 2006, are being appealed.

STATUS OF AMENDMENTS

A Response was submitted on April 7, 2006 in reply to the Final Office Action dated March 29, 2006.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 1 (and similarly in Claims 24 and 31) recites a first memory location being allocated for storing contents to be displayed by a first display device (page 11, lines 21-23; block 406 of Figure 4). The first memory location is accessible by a video display controller (page 9, lines 10-19). In addition, a second memory location is allocated for storing contents to be displayed by a second display device (page 12, lines 17-20; block 418 of Figure 4). Similarly, the second memory location is accessible by the video display controller (page 9, lines 10-19).

In response to a selection of a concurrent display mode, identical information are provided to the first and second memory locations, such that contents displayed on the first display device are identical to contents displayed on the second display device (page 12, lines 2-7; block 414 of Figure 4). In response to a selection of a split display mode, information in the first memory location are retained, and information in the second memory location are updated, such that contents displayed on the first display device are different from contents displayed on the second display device (page 12, lines 15-22; block 422 of Figure 4).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Examiner's rejection of Claims 1-2, 4, 6-7, 24-25, 27, 29-32, 34 and 36-37 under 35 U.S.C. § 103(a) as being unpatentable over *Chee* (US 5,694,141) in view of *Ranganathan* (US 5,764,201).

ARGUMENT

The Examiner's rejections of Claims 1-2, 4, 6-7, 24-25, 27, 29-32, 34 and 36-37 are not well-founded and should be reversed.

I.   The claimed retaining information step is not taught or suggested by *Chee*

Claim 1 (and similarly Claims 24 and 31) recites a step of "in response to a selection of a split display mode, retaining information in said first memory location and updating information in said second memory location, such that contents displayed on said first display device are different from contents displayed on said second display device."

On page 5 of the Final Office Action, the Examiner asserts the claimed step of "retaining information in said first memory location and updating information in said second memory location" is disclosed by *Chee* in col. 17, lines 45-54. Col. 17, lines 45-54 of *Chee* states

> However, the display FIFO's 56 and 56' will be allowed sufficient access to the DRAM 38 that the FIFO's do not run out of display data originating with the particular memory spaces 100' and 102'. Accordingly, although the accesses to the DRAM 38 are intermittent for each of the display FIFO's 56 and 56', the displays 14/24 and 14/24' will each be supplied simultaneously with different display data. That is, the user of the computer system 10 will see a different image presented on the displays 14 and 24 simultaneously.

Apparently, the Examiner characterizes *Chee*'s FIFOs 56 and 56' as the claimed first and second memory locations, respectively. According to *Chee*, "displays 14/24 and 14/24' will each be supplied simultaneously with different display data. That is, the user of the computer system 10 will see a different image presented on the displays 14 and 24 simultaneously." However, the essence of simultaneously displaying different images on different displays does not necessarily mean "retaining information in said first memory location and updating information in said

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second memory location," as claimed. For example, information in both memory locations may be updated to provide the same result, *i.e.*, different images simultaneously displayed on different displays.

Because the claimed invention includes novel features that are not taught or suggested by *Chee*, the § 103 rejection is improper.

II.   The Examiner has not provided any suggestion how the teachings of *Chee* can be reconciled with those of *Ranganathan* to render the claimed invention obvious under § 103

Claim 1 also recites a step of "allocating a first memory location for storing contents to be displayed by said first display device" and "allocating a second memory location for storing contents to be displayed by said second display device." *Ranganathan* discloses the usage of a single memory, such as a memory 56 in Figures 4-8, but does not teach or suggest the claimed allocation of two memory locations.

On page 6 of the Final Office Action, the Examiner asserts that the teachings of the claimed allocation of two memory locations are also come from *Chee*. *Chee* depicts memory locations 100' and 120' along with FIFOs 56 and 56' to display different images on different displays. On the other hand, *Ranganathan* teaches one single memory 56 to provide the same information to be displayed on two different displays. However, the Examiner has not indicated how *Chee*'s teaching of two memory locations can be applied to *Ranganathan*'s teaching of a single memory.

Under MPEP § 2143, in order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art references must teach or suggest all the claimed limitations. The Examiner has not provided any motivation or suggestions as to how *Chee*'s method of displaying

using two memory locations can be reconciled with *Ranganathan*'s method of displaying using only one memory location to render the claimed invention obvious. Since the Examiner has not provided any motivation or suggestion for combining *Chee*'s teaching of two memory locations with *Ranganathan*'s teaching of a single memory location, the *prima facie* case of obviousness is not met.

It is apparent that one of the reasons the Examiner arrived at the above-mentioned assertions is that the Examiner has selectively combined *Chee* and *Ranganathan* to reject the claimed invention, and the Examiner had reconstructed the claimed invention from the prior art by using Appellants' claim as a "blueprint." The Examiner cannot use hindsight to pick and choose among disclosures in the prior art to make the § 103 rejection.

CONCLUSION

For the reasons stated above, Appellants believe that the claimed invention clearly is patentably distinct over the cited reference, and that the rejections under 35 U.S.C. § 103 are not well-founded. Hence, Appellants respectfully urge the Board to reverse the Examiner's rejection.

Respectfully submitted,

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ATTORNEY FOR APPELLANTS

CLAIMS APPENDIX

1.   A method for providing display control on a computer system having a first display device and a second display device, said method comprising:

allocating a first memory location for storing contents to be displayed by said first display device, wherein said first memory location is accessible by a video display controller;

allocating a second memory location for storing contents to be displayed by said second display device, wherein said second memory location is accessible by said video display controller;

in response to a selection of a concurrent display mode, providing identical information to said first and second memory locations, such that contents displayed on said first display device are identical to contents displayed on said second display device; and

in response to a selection of a split display mode, retaining information in said first memory location and updating information in said second memory location, such that contents displayed on said first display device are different from contents displayed on said second display device.

2.   The method of claim 1, wherein said providing identical information further includes providing information from a frame buffer to said first and second memory locations.

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3.   The method of claim 2, wherein said updating information further includes

       allocating a second frame buffer; and

       providing information from said second frame buffer to said second memory location while providing information from said frame buffer to said first memory location.

4.   The method of claim 1, wherein said providing identical information further includes setting a pointer pointing from a frame buffer to said first and second memory locations.

5.   The method of claim 4, wherein said updating information further includes

       allocating a second frame buffer; and

       setting a second pointer pointing from said second frame buffer to said second memory location and setting said pointer pointing from said frame buffer to said first memory location.

6.   The method of claim 1, wherein said first display device is external from said computer system and said second display device is internal to said computer system.

7.   The method of claim 1, wherein said selection between said concurrent display mode and said split display mode are made via a soft key function.

8-23. cancelled.

24.   A computer program product for providing display control on a computer system having a first display device and a second display device, said computer program product comprising:

program code means for allocating a first memory location for storing contents to be displayed by said first display device, wherein said first memory location is accessible by a video display controller;

program code means for allocating a second memory location for storing contents to be displayed by said second display device, wherein said second memory location is accessible by said video display controller;

program code means for providing identical information to said first and second memory locations, in response to a selection of a concurrent display mode, such that contents displayed on said first display device are identical to contents displayed on said second display device; and

program code means for retaining information in said first memory location and updating information in said second memory location, in response to a selection of a split display mode, such that contents displayed on said first display device are different from contents displayed on said second display device.

25.   The computer program product of claim 24, wherein said program code means for providing identical information further includes program code means for providing information from a frame buffer to said first and second memory locations.

26.   The computer program product of claim 25, wherein said program code means for updating information further includes

    program code means for allocating a second frame buffer; and

    program code means for providing information from said second frame buffer to said second memory location while providing information from said frame buffer to said first memory location.

27.   The computer program product of claim 24, wherein said program code means for providing identical information further includes program code means for setting a pointer pointing from a frame buffer to said first and second memory locations.

28.   The computer program product of claim 27, wherein said program code means for updating information further includes

    program code means for allocating a second frame buffer; and

    program code means for setting a second pointer pointing from said second frame buffer to said second memory location and setting said pointer pointing from said frame buffer to said first memory location.

29.   The computer program product of claim 24, wherein said first display device is external from said computer system and said second display device is internal to said computer system.

30.   The computer program product of claim 24, wherein said selections between said concurrent display mode and said split display mode are made via a soft key function.

31.   An apparatus for providing display control on a computer system having a first display device and a second display device, said apparatus comprising:

means for allocating a first memory location for storing contents to be displayed by said first display device, wherein said first memory location is accessible by a video display controller;

means for allocating a second memory location for storing contents to be displayed by said second display device, wherein said second memory location is accessible by said video display controller;

means for providing identical information to said first and second memory locations, in response to a selection of a concurrent display mode, such that contents displayed on said first display device are identical to contents displayed on said second display device; and

means for retaining information in said first memory location and updating information in said second memory location, in response to a selection of a split display mode, such that contents displayed on said first display device are different from contents displayed on said second display device.

32.   The apparatus of claim 31, wherein said means for providing identical information further includes means for providing information from a frame buffer to said first and second memory locations.

33.   The apparatus of claim 32, wherein said means for updating information further includes

means for allocating a second frame buffer; and

means for providing information from said second frame buffer to said second memory location while providing information from said frame buffer to said first memory location.

34.   The apparatus of claim 31, wherein said means for providing identical information further includes means for setting a pointer pointing from a frame buffer to said first and second memory locations.

35.   The apparatus of claim 34, wherein said means for updating information further includes

means for allocating a second frame buffer; and

means for setting a second pointer pointing from said second frame buffer to said second memory location and setting said pointer pointing from said frame buffer to said first memory location.

36.   The apparatus of claim 31, wherein said first display device is external from said computer system and said second display device is internal to said computer system.

37.   The apparatus of claim 31, wherein said selections between said concurrent display mode and said split display mode are made via a soft key function.

EVIDENCE APPENDIX

Not applicable.

RELATED PROCEEDINGS APPENDIX

Not applicable.